

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
BEDWELL, RYAN D. et al.

Application No.: 10/675005

Filed: September 30, 2003

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Patent No.: 6917555 B2

Issue Date: July 25, 2005

Examiner: Son T. Dinh

Group Art Unit: 2824

Docket No.: SC12942TH

Title: INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE
CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR

Certificate of Submission

I hereby certify that this correspondence is being submitted to the
U.S.P.T.O., Alexandria, VA.

___ Addressed per C.F.R. § 1.1(a) and deposited with the United States
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XX Submitted electronically via EFS in accordance with "Legal
Framework for EFS-Web".

2.22.2007

Date of Submission

Pat Thomas

Signature

Pat Thomas

Printed Name of Person Signing Certificate

Commissioner for Patents
Alexandria, VA 22313

SUBMISSION OF CERTIFICATE OF CORRECTION

Dear Commissioner:

Enclosed is a Certificate of Correction listing error(s) in the subject patent. Please enter these corrections. Since the errors appear to be on the part of the Applicant, please charge the required fee to Deposit Account 503079, Freescale Semiconductor, Inc.

02/26/07
Date

Respectfully submitted,

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CERTIFICATE OF CORRECTION

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PATENT NO.: 6917555 B2
APPLICATION NO: 10/675005
DATE: July 12, 2005
INVENTOR(S): BEDWELL, RYAN D. et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 12, Line 21, Claim No. 21:

Change "plan" to - -plane- -.

MAILING ADDRESS OF SENDER (Please do not use customer number below)

Freescale Semiconductor, Inc.
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Austin, TX 78729